What is claimed is:

1. A method of accessing a memory resource, comprising:

processing a first instruction in an instruction pipeline, wherein the first instruction requires access to the memory resource;

processing a second instruction in the instruction pipeline while the first instruction is being processed, wherein the second instruction requires access to the memory resource; and

updating the memory resource to prevent a data hazard based on an order of receipt of a first instruction response and a second instruction response.

2. The method of claim 1, wherein updating the memory resource to prevent the data hazard based on the order of receipt of the first instruction response and the second instruction response includes not writing returned data associated with the first instruction response in response to receipt of the first instruction response subsequent to receipt of the second instruction response.

3. The method of claim 1, wherein updating the memory resource to prevent the data hazard based on the order of receipt of the first instruction response and the second instruction response includes storing logical values in a data structure containing pendency information associated with the memory resource.

4. The method of claim 3, wherein storing the logical values in the data structure containing pendency information associated with the memory resource includes at least one of setting and resetting tracking bits associated with the memory resource.

5. A method of managing access to a memory resource, comprising:

storing first tracking information in response to a first instruction requiring access to the memory resource;

storing second and third tracking information in response to a second instruction requiring access to the memory resource; and

managing access to the memory resource by changing the first, second and third tracking information in one of a plurality of sequences based on an order of receipt of a first instruction response and a second instruction response.

6. The method of claim 5, wherein storing the first, second and third tracking information includes storing one of first and second logical states in respective first, second and third tracking bits.

7. The method of claim 6, wherein storing the one of the first and the second logical states in the respective first, second and third tracking bits includes setting the first, second and third tracking bits.

8. The method of claim 5, wherein changing the first, second and third tracking information in one of the plurality of sequences includes storing one of first and second logical states in respective first, second and third tracking bits.

9. The method of claim 8, wherein storing the one of the first and second logical states in the respective first, second and third tracking bits includes resetting the first, second and third tracking bits.

10. The method of claim 5, wherein changing the first, second and third tracking information in one of the plurality of sequences includes changing the first and third tracking information prior to changing the second tracking information in response to receiving the second instruction response prior to receiving the first instruction response.

11. A method of managing access to a memory register, comprising:

establishing a data structure that includes pendency information associated with the memory register;

receiving a first instruction that requires access to the memory register;

storing first information associated with a primary pendency of the memory register in the data structure;

receiving a second instruction that requires access to the memory register;

storing second information associated with a secondary pendency of the memory register in the data structure; and

changing the first and second information stored in the data structure based on an order of receipt of a first data return associated with the first instruction and a second data return associated with the second instruction.

12. The method of claim 11, wherein establishing the data structure that includes pendency information associated with the memory register includes establishing at least one of a table and a scoreboard that includes the first and second information.

13. The method of claim 12, wherein the step of establishing the at least one of the table and the scoreboard that includes the first and second information includes establishing a first tracking bit associated with the primary pendency of the memory register and second and third tracking bits associated with the secondary pendency of the memory register.

14. The method of claim 11, wherein storing the first information associated with the primary pendency of the memory register in the data structure includes setting a first bit in the data structure.

15. The method of claim 14, wherein storing the second information associated with the secondary pendency of the memory register in the data structure includes setting second and third bits in the data structure.

16. The method of claim 11, wherein changing the first and second information stored in the data structure based on the order of receipt of the first and second data returns includes logically inverting the first information and logically inverting a portion of the second information.

17. A method of controlling access to a memory register, comprising:

establishing a data structure that is adapted to contain primary and secondary pendency information associated with the memory register;

receiving a first instruction in an instruction pipeline, wherein the first instruction requires access to the memory register;

storing first information associated with a primary pendency of the memory register in the data structure;

receiving a second instruction in the instruction pipeline, wherein the second instruction requires access to the memory register;

storing second information in the data structure associated with a secondary pendency of the memory register; and

changing the first and second information stored in the data structure based on an order of receipt of first and second responses corresponding to the respective first and second instructions.

18. The method of claim 17, wherein establishing the data structure that is adapted to contain the primary and secondary pendency information associated with the memory register includes establishing a plurality of memory bits, each of which corresponds to one of the primary and secondary pendency information.

19. The method of claim 17, wherein changing the first and second information stored in the data structure based on the order of receipt of the first and second responses includes changing a first logical value of a first memory location within the data structure that is associated with the secondary pendency of the memory register prior to changing a second logical value of a second memory location within the data structure that is associated with the secondary pendency of the memory register.

20. A system for managing access to a memory resource, comprising:

a memory resource tracking information database to contain primary and secondary pendency information associated with the memory resource;

a memory resource access detector to change at least one of the primary and the secondary pendency information in response to instructions requiring access to the memory resource;

a data return detector to change at least one of the primary and the secondary pendency information based on an order of receipt of data returns; and

a memory resource update unit to use at least one of the primary and secondary pendency information to update the memory resource to prevent a data hazard.

21. The system of claim 20, wherein the memory resource tracking information database is a scoreboard including a plurality of tracking bits associated with the memory resource.

22. The system of claim 20, wherein the memory resource update unit uses the at least one of the primary and secondary pendency information to determine an order of receipt of instruction responses for use in preventing the data hazard.

23. A memory management system, comprising:

a computer readable memory; and

a processing unit having an instruction pipeline, wherein the processing unit is adapted to receive first and second instructions in the instruction pipeline that each require access to the computer readable memory, wherein the processing unit is further adapted to store primary and secondary pendency information in a data structure in response to receipt of the first and second instructions in the instruction pipeline and wherein the processing unit is further adapted to change the primary and secondary pendency information stored in the data structure based on an order of receipt of primary and secondary data returns that correspond to the respective first and second instructions.

24. The system of claim 23, wherein the processing unit is further adapted to establish the data structure to include a plurality of bits, each of which is associated with one of the primary and secondary pendency information.

25. The system of claim 23, wherein the processing unit is further adapted to change the primary and secondary pendency information stored in the data structure based on the order of receipt of the primary and secondary data returns by changing a first logical value of a first memory location of the data structure prior to changing a second logical value of a second memory location of the data structure.

26. The system of claim 23, wherein the data structure is one of a table and a scoreboard including a plurality of bit fields corresponding to the primary and secondary pendency information.

27. The system of claim 23, wherein the processing unit is further adapted to tag each of the first and second instructions to identify the first and second instructions as being one of a primary access and a secondary access.

28. A software routine stored on a computer readable memory and adapted to be executed by a processor, the software routine comprising:

first software that establishes a data structure adapted to contain primary and secondary pendency information associated with a memory resource;

second software that receives a first instruction in an instruction pipeline, wherein the first instruction requires access to the memory resource;

third software that stores first information associated with a primary pendency of the memory resource in the data structure in response to receipt of the first instruction;

fourth software that receives a second instruction in the instruction pipeline, wherein the second instruction requires access to the memory resource;

fifth software that stores second information associated with a secondary pendency of the memory resource in the data structure; and

sixth software that changes the first and second information stored in the data structure based on an order of receipt of first and second responses corresponding to the respective first and second instructions.

29. The system of claim 28, wherein the first software is further adapted to establish the data structure to include a plurality of memory bits, each of which is associated with one of the primary and secondary pendency information.

30. The system of claim 28, wherein the sixth software is further adapted to change the first and second information stored in the data structure based on the order of receipt of the first and second responses by changing a first logical value of a first memory location within the data structure that is associated with the secondary pendency of the memory resource prior to changing a second logical value of a second memory location within the data structure that is associated with the secondary pendency of the memory resource.